Remarks/Arguments

The Office Action of December 22, 2004 and the references cited therein have been carefully studied and reviewed, and in view of the foregoing Amendment and following representations, reconsideration is respectfully requested.

1. The Rejection of Claim 11 Under 35 USC 103 As Being Unpatentable Over Bohr (USP 5,536,675) in View of Chang et al. (USP 6,326,310) and Wu (USP 6,165,854).

None of the references teach Applicants' claimed use of the same sidewall spacer as a mask during a series of etching steps.

Claim 11 has been amended to incorporate therein the subject matter of canceled claim 12. Thus, claim 11, as now amended, includes steps of (1) etching a portion of a semiconductor substrate using a hard mask pattern 106, 108 and a sidewall spacer 110 as a mask to thereby form a shallow trench 112 (FIG. 9), (2) forming a thermal oxide layer 114 along inner walls of the semiconductor substrate that define opposed side walls and a bottom wall of the shallow trench (FIG. 10), and (3) with the same spacer 110 used to form the shallow trench exposed, etching the resulting structure using the hard mask pattern and said spacer as a mask to extend to extend the shallow trench deeper into the semiconductor substrate.

Bohr discloses a method in which a deep trench 242 (FIG. 3D) is formed by (1) etching a portion of a semiconductor substrate using a hard mask pattern 210, 220 and a photoresist pattern 230 as a mask to thereby form a shallow trench 242a (FIG. 3A), (2) forming a thermal oxide layer 252a along inner walls of the semiconductor substrate that define opposed side walls and a bottom wall of the shallow trench (FIG. 3B), and (3) etching the resulting structure using a patterned photoresist layer 231 as a mask to extend the shallow trench deeper into the semiconductor substrate.

As admitted by the Examiner, Bohr fails to disclose the use of any sidewall spacer as an etching mask. More particularly, as distinguished from Applicants' method, as is now claimed, Bohr does not disclose or suggest the use a sidewall spacer in common to both form the shallow trench 242a, and to extend the shallow trench deeper after the thermal oxide layer 252 is formed.

Chang et al. teach a method of forming a "shallow" trench isolation using sets of sidewall spacers 208, 210 and 212, 214 **formed one after another** as etching masks to impart a desired profile , e.g., an inclined profile, to the "shallow" trench. More specifically, in Chang et al., spacer set 208, 210 is used as a mask during an initial phase of etching (FIG. 4A – 4B). However, during the subsequent phase of etching (FIG. 4B – 4C), that very same spacer set 208, 210 is not exposed; rather, spacer set 208, 210 is covered by new spacer set 212, 214 so that the trench can be

narrowed. Thus, Chang et al. fails to teach anything corresponding to Applicant's claimed step (e), namely the step of forming the deep trench while the same spacer used to form the shallow trench is exposed.

The reference to Wu was relied on by the Examiner for the teachings therein associated with SiON layer 12, and thus does not overcome the deficiencies in the Bohr and Chang et al. references described above.

That is, none of the references teach a technique in which the same sidewall spacer (or spacer set) is used to form a shallow trench in a first etching process, and then is also exclusively used to extend the shallow trench deeper in a second etching process. Accordingly, the references can not render obvious the subject matter of Applicants' claimed 11, particularly with respect to steps (c), (d) and (e) recited therein.

2. The Rejection of Claims 23 and 24 Under 35 USC 103 As Being Unpatentable Over Bohr (USP 5,536,675) in View of Chang et al. (USP 6,326,310) and Wu (USP 6,165,854).

Claim 23 has been amended so as to be in independent form.

Claims 23 and 24 thus now each set forth steps of (c) etching the semiconductor substrate **to thereby form a shallow trench** 112, (d) **forming a thermal oxide layer** 114 **along inner walls** of the semiconductor substrate **that define** opposed side walls and **a bottom wall of the shallow trench 112,** and (e) removing the **entire** portion of the thermal oxide layer 114 (FIG. 10) that is disposed along the bottom of the shallow trench 112 by etching to extend said shallow trench deeper into the semiconductor substrate and thereby **form a deep trench** 116 (FIG. 11) **that has substantially the same width as the shallow trench 112.**

Bohr fails to disclose such steps.

In the illustrated embodiments of Bohr, **only a portion** of the oxide layer 252a lying along the bottom of the shallow trench 242a is removed, and the **deep trench** 242b (FIG. 3C) is formed to have **a width that is much smaller than that of the shallow trench 242a** (FIG. 3B).

The Examiner also refers to col. 6, lines 20 – 25; col. 6, lines 49 – 65; and col. 7, lines 9-18).

At col. 6, lines 20 – 25, Bohr only discloses that the width of the deep trench may "vary" as desired. As an example, Bohr states that the deep trench need only be wide enough to provide "adequate" isolation in CMOS circuits. It would be appreciated that this is suggestion only of making the deep trench narrower than what is shown and not as wide as the shallow trench. That is, those of ordinary skill in the

art would know that a deep trench for isolating CMOS devices is significantly narrower than the shallow trenches known for isolating bipolar devices, for example. Accordingly, this passage in Bohr is not suggestive of forming the deep trench 242b to be of the same width as the shallow trench 242a.

At col. 6, lines 49 – 65, Bohr acknowledges that the steps of his process can be reordered or other processing steps can be used, etc. "as long as the end result is the formation of shallow trench **241** and deep trench **242**". However, in this passage, Bohr only speaks of the deep trench 242 as part of a **T-shaped** deep trench isolation structure. Accordingly, there is nothing in this passage to suggest that the deep trench 242b can have the same width as the shallow trench 242a.

On the other hand, at col. 7, lines 9 – 18, the Examiner is correct in noting that Bohr mentions a deep trench isolation structure in which only a deep narrow trench similar to trench 242b is formed. However, in this case, "shallow trench 242a is not formed **at all**" (emphasis supplied). Thus, the method of this disclosed embodiment would lack Applicants' claimed steps of (c) etching the semiconductor substrate **to thereby form a shallow trench** 112, and (d) **forming a thermal oxide layer** 114 **along inner walls** of the semiconductor substrate **that define** ... **a bottom wall of the shallow trench 112.**

Chang et al. also fails to disclose such steps. In fact, Chang et al. teaches away from Applicants' invention of claims 23 and 24. The entire purpose of the Chang et al. method is to achieve a profiling wherein the deeper portions of the trench have widths that are significantly different from those of the shallower portions.

Again, Wu was merely relied on by the Examiner for the teachings therein associated with SiON layer 12, and thus does not overcome the deficiencies in the Bohr and Chang et al. references described above.

Therefore, the references can not render the subject matter of Applicant's claims 23 and 24 obvious under 35 USC 103 because the references do not suggest at least steps (c), (d) and (e) of the claims.

3. The Rejection of Claim 17 Under 35 USC 103 As Being Unpatentable Over Madan (USP 5,3350,941) in View of Wu (USP 6,165,854).

It is axiomatic that to establish a *prima facie* case of obviousness, based on a combination of references under 35 USC 103, the Examiner must identify suggestion that would have motivated one of ordinary skill in the art to have modified the references.

The Examiner finds that one of ordinary skill in the art would have been motivated to have modified the method of Madan to incorporate the buffer layer of Wu "in order to prevent parasitic leakage".

The Examiner has not established a *prima facie* case of obviousness because there is no suggestion that would have motivated one of ordinary skill in the art to have combined the references for the reason proposed by the Examiner.

Parasitic capacitance may occur as a so-called corner effect in trench isolation structures when the corner of the trench is sharp. Please refer to col. 2, lines 1 -10 of the Wu reference and, especially to USP 5, 521,422 referred to thereat.

Although the Examiner is correct in noticing that the Madan reference refers to parasitic capacitance as a problem at col. 1, lines 15 – 30, this portion of the Madan specification refers to parasitic capacitance being a problem in prior art devices **not in the Madan device**.

To the contrary, Madan discloses a trench isolation method in which bird's beak regions 26a, 26b, 28a, and 28b are formed at the sidewalls of trenches 34, 36 and 38 (FIG. 1e) to round the corners of the trenches. Hence, little, if any, parasitic leakage would occur at the corners **in the Madan device**. Any spurious leakage is prevented by the provision of channel stop regions 60.

Wu teaches another means of rounding the corners of the trenches. In the method taught by Wu, trenches 8 are formed using a hard mask pattern 4 (FIG. 3). The hard mask 4 is then removed to expose the substrate 2. Subsequently, the corners of the trenches 8 are rounded by depositing a layer of SiON directly on the exposed substrate to thermally process the substrate 2 (col. 4, lines 7 – 14).

Applicants most strenuously assert that there is simply no suggestion from the references to add the SiON layer of Wu to the structure disclosed by Madan after the trenches 34, 36 of Madan are formed as shown in FIG. 1e. As was previously mentioned, the corners of the substrate 10 **of the Madan device have already been rounded** by the LOCOS structure 28 which, when etched, yields the resulting bird's beak regions 26b, 28a, and 28b. Therefore, adding the SiON layer **would not** serve "to prevent parasitic leakage" in the Madan device because there would no significant parasitic capacitance to begin with.

In other words, the methods disclosed by Madan and Wu would clearly be viewed by those of ordinary skill in the art as **alternative** techniques of rounding the corners of the substrates at the tops of the trenches to reduce parasitic capacitance. Accordingly, the rejection should be withdrawn.

For the foregoing reasons as to why the references either do not teach particular aspects of Applicants' claims or as to why there is no suggestion that would have motivated one of ordinary skill in the art to have combined the references, it seen that the references do not render Applicants' claims obvious under 35 USC 103. Accordingly, early reconsideration and allowance of the claims are respectfully requested.

Respectfully submitted,

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